WHAT IS CLAIMED IS:

1. A semiconductor circuit comprising:

a first voltage relaxation circuit coupled between first and second nodes, the first node receiving a first potential;

a second voltage relaxation circuit coupled between third and fourth nodes, the third node receiving said first potential;

a first charge pump circuit with an output thereof coupled to the second node;

a second charge pump circuit with an output thereof coupled to the fourth node;

a third charge pump circuit with an output thereof coupled to the first charge pump;

a fourth charge pump circuit with an output thereof coupled to the second charge pump;

a first rectifier MOSFET with a source-drain path thereof coupled between the second node and a fifth node; and

a second rectifier MOSFET with a source-drain path thereof coupled between the fourth node and said fifth node,

wherein the first charge pump circuit outputs a first signal which varies between a high level and a low level alternately and periodically,

wherein the second charge pump circuit outputs a second signal which varies between a high level and a low level alternately and periodically, the high level of the second

signal being equal to the high level of the first signal,

wherein the third charge pump circuit outputs a third signal which varies between a high level and a low level alternately and periodically, the high level of the third signal being lower than the high level of the first signal, and

wherein the fourth charge pump circuit outputs a fourth signal which varies between a high level and a low level alternately and periodically, the high level of the fourth signal being equal to the high level of the third signal.

2. A semiconductor circuit according to claim 1,

wherein the first voltage relaxation circuit comprises first and second MOSFETs having their source-drain paths coupled in series between the first and second nodes, and

wherein the second voltage relaxation circuit comprises third and fourth MOSFETs having their source-drain paths coupled in series between the third and fourth nodes.

3. A semiconductor circuit according to claim 2,

wherein the first and second MOSFETs have the same channel conductivity type, and wherein the third and fourth MOSFETs have the same channel conductivity type.

4. A semiconductor circuit according to claim 2,

wherein the gate of the first rectifier MOSFET is coupled to the second charge pump circuit,

wherein the gate of the second rectifier MOSFET is

coupled to the first charge pump circuit, and

wherein the gates of the first and second rectifier MOSFETs receive a complementary voltage.

5. A semiconductor circuit according to claim 4,

wherein a gate of the first MOSFET is controlled by a fifth signal,

wherein a gate of the third MOSFET is controlled by a sixth signal, and

wherein gates of the second and fourth MOSFETs are commonly coupled.

6. A semiconductor circuit according to claim 4,

wherein the high level of the first and second signals, respectively, is three times the magnitude of the first potential, and

wherein the high level of the third and fourth signals, respectively, is twice the magnitude of the first potential.

7. A semiconductor circuit according to claim 4,

wherein the first and second rectifier MOSFETs have the same conductivity type, and

wherein the first MOSFET has a different conductivity type from the first rectifier MOSFET.

8. A semiconductor circuit according to claim 4, further comprising:

a plurality of word lines, a plurality of bit lines, and a plurality of memory cells coupled to the plurality of word lines and bit lines; and

a row decoder for selecting ones of said plurality of word lines,

wherein said row decoder receives a voltage corresponding to the output of the first and second rectifier MOSFETs.

9. A semiconductor circuit according to claim 8,

wherein said plurality of memory cells are dynamic random access memory (DRAM) cells.

10. A semiconductor circuit according to claim 4,

wherein when the first signal is at said high level, the second signal is at said low level, and when the first signal is at said low level, the second signal is at said high level.

11. A semiconductor circuit according to claim 2,

wherein said first through fourth MOSFETs have the same channel conductivity type, and

wherein the first and second rectifier MOSFETs have a channel conductivity type opposite that of the first through fourth MOSFETs, respectively.

12. A semiconductor circuit comprising:

a voltage generating circuit including a first node, a second node and a third node, the first node being supplied with a first potential, the second node being supplied with a second potential, lower than the first potential, and said voltage generating circuit outputting a third potential, higher than the first potential, to the third node,

wherein the voltage generating circuit further includes: first and second MOSFETs coupled in series between a fourth node and a fifth node; and a first charge pump circuit coupled to the fourth node,

wherein the first potential is supplied to the fifth node,

wherein the first charge pump circuit outputs a first signal which varies between a high level and a low level, alternately, the high level of the first signal being higher than the first potential, and

wherein a gate of the first MOSFET receives a second signal which varies between a high level and a low level, alternately, the high level of the second signal being lower than the high level of the first signal.

13. A semiconductor circuit according to claim 12, further comprising:

a plurality of dynamic memory cells provided on intersections between a plurality of word lines and a plurality of bit lines; and

a plurality of sense amplifiers coupled to said plurality of bit lines,

wherein when one of said plurality of word lines is selected, that word line is driven to the third potential from the voltage generating circuit.

14. A semiconductor circuit according to claim 12,

wherein said voltage generating circuit further includes:

a rectifier MOSFET; and a second charge pump circuit coupled to the rectifier MOSFET,

wherein the second charge pump circuit outputs a third signal which varies between a high level and low level, alternately, the high level of the third signal being equal to the high level of second signal,

wherein the third signal is supplied to the third node via the rectifier MOSFET, and

wherein a gate of the rectifier MOSFET is coupled to the fourth node.

15. A semiconductor circuit according to claim 14,

wherein the second charge pump circuit is coupled to the gate of the first MOSFET, and

wherein the third signal is equal to the second signal.

16. A semiconductor integrated circuit device according to claim 15,

wherein the voltage generating circuit further includes a third charge pump circuit coupled to the first charge pump circuit and the gate of the first MOSFET,

wherein the third charge pump circuit outputs the second signal to the first charge pump circuit and the gate of the first MOSFET.

17. A semiconductor integrated circuit according to claim 16,

a plurality of dynamic memory cells provided on intersections between a plurality of word lines and a plurality of bit lines; and

a plurality of sense amplifiers coupled to said plurality of bit lines,

wherein when one of said plurality of word lines is selected, that word line is driven to the third potential from the voltage generating circuit.

18. A semiconductor circuit comprising:

a voltage boosting circuit for providing an output voltage having at least three times the amplitude of an input voltage thereof; and

a voltage relaxation circuit coupled between the output of the voltage boosting circuit and a first node for receiving a first potential,

wherein the voltage boosting circuit comprises a plurality of charge pump circuits, and

wherein the voltage relaxation circuit comprises a plurality of MOSFETs coupled in series between the first node and the output of the voltage booster circuit.

19. A semiconductor circuit according to claim 18,

wherein each of the plurality of charge pump circuits includes a capacitor and a node fed with pulses.

20. The semiconductor circuit according to claim 19,

wherein the plurality of MOSFETs are series-coupled via their source-drain paths thereof and have the same channel conductivity type.